REMARKS

Claims 131-146 are currently pending. Claim 139 is amended. The claims, as amended, are reproduced in the appendix for sake of convenience.

Claims 131-138, and 142-146 were rejected under 35 U.S.C. §112, ¶1. Claims 139-141 were rejected under 35 U.S.C. §102(b) as anticipated by "Predecoding Mechanism for Superscalar Architecture" by Minagawa et al. (Minagawa).

In light of the following remarks and submissions, the undersigned respectfully requests withdrawal of the rejections. Further, the undersigned respectfully requests that an interference be declared under 37 C.F.R. §1.607 between the present application and the '065 patent, as requested in the previous amendment.

I. Formal Matters

Claims 131-138, and 142-146 were rejected under 35 U.S.C. §112, ¶1. Specifically, the Examiner asserted that the specification fails to disclose providing "a separate template field within the instruction bundle." The undersigned respectfully traverses this rejection for at least two non-exclusive reasons. First, the specification discloses embodiments where template bits are contiguous, sequential and/or not separated. Second, in the industry, the term "field" does not require bits to be contiguous, sequential and not separated.

A. Specification Supports "field"

It is asserted that the following passages in the specification explicitly disclose an embodiment where template bits are contiguous, sequential, and/or not separated. For example, the specification discloses an embodiment where some of the template bits are combined and placed in an instruction location in the frame. In particular, the specification states on p. 7, lines 10-13:

> **In this case, in another embodiment, the pipeline identifier information is supplied on a different clock cycle, then combined with the instructions in the cache ...Emphasis added.**

This is done by "blanking" out one instruction in the cache:

> **Such an approach can be achieved by adding a "no-op" instruction ...p. 7, lines 14-15. Emphasis added.**

The pipeline identifiers are then placed at the location of the "no-op" instruction:

> ... **with fields that identify the pipeline for execution of the instruction, or by supplying the information relating to the parallel instructions in another manner. p. 7, lines 15-18. Emphasis added.**

As seen in Fig. 3, instructions W0:W7 are included in a frame of instructions. According to the alternative embodiment described above, initially one of the instructions, for example W0, includes a "no-op" instruction. Next, according to this embodiment, the pipeline identifiers for instructions W1:W7 are placed at location W0. Of course, W0 does not need a pipeline identifier for it was a "no-op" instruction, Thus the pipeline identifiers in W0 are then used to identify appropriate pipelines for the other instructions W1:W7. Because the pipeline identifiers for instructions W1:W7 are grouped together at location W0 in the frame, the pipeline identifiers in W0 form a "field."

Accordingly, in view of the above, it is asserted that the term "field" is supported in the specification. The rejections under 35 U.S.C. §112, ¶1 are thus traversed.

B. Industry Definition and Usage of "field"

Attached to this amendment are four attachments that demonstrate that in this industry, the term "template field", or more specifically "field," does not require that the bits are contiguous, sequential, or not separated.

1. Attachment 1

Attachment 1 is a portion of the McGraw-Hill Dictionary of Electronics and Computer Technology © 1984. According to this dictionary, the term "field" does not require that bits be contiguous, sequential, not-separated, or otherwise. In particular, the definition states a field is:

> **A specified area, such as a group of card columns or a set of bit locations in a computer word, used for a particular category of data. Emphasis added.**

2. Attachment 2

Attachment 2 is a portion of the IEEE Standard Dictionary of Electrical and Electronics Terms © 1972. According to this dictionary, in this art, the term "field" does not require that bits have any special relation to each other, i.e., contiguous, or the like. In particular, the dictionary states that a field is:

> **A specified area used for a particular category of data, for example, a group of card columns used to represent a wage rate or a set of bit locations in a computer word, used to express the address of the operand. Emphasis added.**

3. Attachment 3

Attachment 3 is a portion of a Pentium™ Processor User's Manual, Volume 3: Architecture and Programming Manual © 1993. In this manual, descriptions of particular data structures are discussed in depth. Some of these descriptions of the data structures use the term "field" consistent with the above dictionary definition. That is, data structures that include non-contiguous, non-sequential bits, and/or separated bits in a word can be called either "fields" or a "field."

As an example, on page 11-12, Figure 11-8, a "segment limit" "field" is illustrated as bits 19:16 of an upper portion of a word and bits 15:0 of a lower portion of a word. Also see page 12-3, Figure 12-1. On page 11-12, under the "Limit" definition, the manual describes that, "The processor puts together the two limit fields to form a 20-bit value." Importantly, the manual also describes this 20-bit value as a "limit field." For example, on page 11-13, the definition of Limit continues:

> **Expand-down segments reverse the sense of the Limit field; ... This is done to allow segments to be created in which increasing the value held in the Limit field allocates new memory ...Emphasis added.**

Other examples of the 20-bit value being termed a "limit field" include the definition of "Granularity bit" on page 11-12:

Granularity bit: Turns on scaling of the limit field by a factor of 4096 (2^12). ... Also note that only the limit field is affected. Emphasis added.

Another example is illustrated on page 12-5 in section 12.2.2 Limit Checking:
The Limit field of the segment descriptor prevents programs from addressing outside the segment...
While the G bit is clear, the limit is the value of the 20-bit Limit field in the descriptor. When the G bit is set, the processor scales the value in the Limit field by a factor of 2^12. ... Emphasis Added.

4. Attachment 4

Attachment 4 is a portion of an IA-32 Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide © 2000. As can be seen, this guide includes a similar description and usage of the term "limit field" as in the 1993 manual (attachment 3). Additionally, this guide explicitly defines the term "limit field" on Page 4-2.

Limit field – (Bits 0 through 15 in the first doubleword and bits 16 through 19 of the second doubleword of a segment descriptor.)
Determines the size of the segment, along with the G flag and E flag (for data segments). Emphasis added.

Although this guide is after the filing date of the present invention, attachment 4 confirms that the term "limit field" in attachment 3 refers to non-contiguous, non-sequential, and separated bits in a word.

5. Definition and Usage

In light of the above, it is respectfully asserted that the term "field" be interpreted in the claims in this application the same way it is understood in the industry. As illustrated above, the technical dictionaries *do not require* that bits within a "field" be contiguous, sequential, or not separated. The definitions merely require that the "field" represent related data. Further, as demonstrated in the Pentium™ manual, the Industry

explicitly used the term "field" to refer to non-contiguous, non-sequential, and separated bits in a word. The term "field" is thus defined to include non-contiguous, non-sequential, or separate bits in a word.

As we discussed, the "template" portion of the term "template field" only refers to the "particular category of data" (according to the dictionary definition) of the field. In the Pentium™ manual, the "particular category of data" of the field related to "segmentation limit" data. In the present case, the field relates to a "category of data" comprising "template" data. This template data is described in the claims as "specifying a mapping of the instruction slots to the execution unit types." Thus, nothing in the term "template" requires contiguous, sequential, or non-separated data, anymore than "limit field" does in the case of the Pentium™ manual.

Accordingly, in view of the industry definition of the term "field", and industry usage of the term "field," it is asserted that the term "template field" in the above-mentioned claims are supported by the present patent specification. The rejections under 35 U.S.C. §112, ¶1 are thus traversed.

II. The Cited Art Distinguished

Claims 139-141 were rejected under 35 U.S.C. §102(b) as anticipated by "Predecoding Mechanism for Superscalar Architecture" by Minagawa et al. (Minagawa). In light of this rejection, claim 139 has been amended to add additional distinguishing limitations over Minagawa. In particular, the limitation of wherein the routing data is not primarily determined by hardware was added. As can be seen, Minagawa relies only upon on hardware circuits and components to determine Priority Field and Resource Field data. Accordingly, Minagawa does not disclose all the limitations recited in claim 139, and Minagawa does not anticipate claim 139. Claims 140 and 141 are also not anticipated for this reason, and for the specific limitations they recite.

CONCLUSION

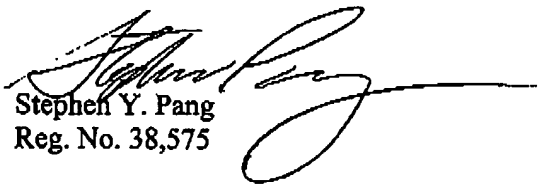
In view of the above, applicant believes the rejections under §112, ¶1, and §102(b) have been overcome. Accordingly, Applicant respectfully requests that the Examiner declare an interference with the previously mentioned '065 patent. Furthermore, the applicant

requests that the examination of the present application be conducted with special dispatch, per 37 C.F.R. §1.607(b).

The Examiner is invited to review the documents cited in the attachments in their entirety. If the Examiner does not have access to such references, the undersigned can provide copies to the Examiner, upon request.

The Examiner is kindly invited to contact the undersigned at the telephone number listed below to discuss any issues the Examiner may have.

Respectfully submitted,



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